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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,529	06/05/2006	Stephan Bolz	S4-03P04584	5910

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EXAMINER	
CLARK, CHRISTOPHER JAY	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,529	BOLZ ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER J. CLARK	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed January 16, 2008 have been fully considered but they are not persuasive.

2. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Williams teaches that a MOSFET is protected between its gate and source with a clamping arrangement of diodes and receives a triggering signal received at its gate. Gscheidle teaches that the MOSFET (T2) of the protection circuit also relies on a voltage clamp between its gate and source and receives a triggering signal via two resistors R3 and R4. Williams teaches a similar setup in which two resistors (Rl and Rs) are used in the gate triggering path with the addition of diode D1. Williams explains in lines 25-36 of Column 7 and in Figures 9A-C that by having such a two resistor/diode configuration in the gate triggering path allows for gate voltage to fall much faster during removal of a triggering signal and to rise at a slower rate to prevent any ringing and overshooting during initiation of a triggering signal. Based on Williams teachings, it should be clear to one skilled in the art that it does not matter the order in series of the resistor that the diode is placed with, only the value of the resistance. Therefore, one skilled in the art would find it reasonable to apply a diode across R4 of Gscheidle

in a manner to replicate the gate triggering path as taught by Williams due to the fact that both are concerned with providing an activation signal to a MOSFET, and one skilled in the art would find it beneficial to utilize the diode as taught by Williams in order to achieve the aforementioned triggering start and stop timing characteristics.

3. Upon the modification of Gscheidle with Williams, in the event that T1 is turned on to remove the triggering signal from T2, the current will flow through the acquired diode as taught by Williams and reach the node at which the collector of T1 and R3 join. The current will divide at this node based on the simple principles of Kirchhoff's current law with the majority of current flowing through T1 and with the remaining amount of current flowing through R3 to the accumulator (Ubatt).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 7-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gscheidle (U. S. Patent 6,031,705) in view of Williams (U. S. Patent 6,172,383).

3. In re Claim 7, Gscheidle teaches a device for protecting an electronic module disposed in a control device in a multi-voltage on-board electrical system having an accumulator with a low on-board electrical system voltage against short circuiting to a high on-board electrical system voltage as seen in Figure 1, comprising:

- a MOSFET (T2) transistor having a drain source path inserted between a control device connection (Ue1) and a connection of the electronic module (Ua1), and with:
    - a source connected to the connection of the electronic module
    - a drain connected to the control device connection
    - a gate
- a Zener diode (D5) connected between said gate and said source of said MOSFET transistor
- a gate resistor (R4) connected between said gate of said MOSFET transistor and a positive pole of the first accumulator (Ubatt)

4. The teaching of Gscheidle does not teach a diode connected in parallel with the gate resistor.

5. Williams teaches as seen in Figures 8A-D that it is known to connect a diode across a gate resistor to allow the voltage to fall much faster during removal of a triggering signal and to rise at a slower rate to prevent any ringing and overshooting during initiation of a triggering signal (Column 7 Lines 25-36).

6. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the gate diode as taught by Williams in order to turn off the protective transistor more rapidly when a fault voltage is detected and thus reduce the risk of damage to the protected circuitry while turning on the protective transistor at a slower rate to prevent any ringing and overshooting.

7. The examiner would like to note that neither the teaching of Gscheidle or Williams specifically teach implementing the protective device as discussed thus far in a multi-voltage

system. Upon their combination, they do possess all of the structural elements as claimed and are therefore considered capable of matching the intended use of being used in a multi-voltage system.

8. In re Claim 8, Gscheidle teaches that the electronic module is disposed in control device for controlling low-power consumers or for processing/transmitting data (Column 1 Lines 15-47).

9. In re Claim 9, Gscheidle teaches that Zener diode is configured with a breakdown voltage lower than a maximum permitted gate source voltage of said MOSFET transistor (Column 3 Lines 55-57).

10. In re Claim 10, Gscheidle as modified by Williams discloses the claimed invention except for the source voltage of the transistor being specifically limited to a value which is the difference of the accumulator voltage and the threshold voltage. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to limit the source voltage of the transistor (which is also the voltage being supplied to the protected circuitry) to a value that will not harm the circuitry being protected since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

11. In re Claim 11, Gscheidle teaches that upon detection of an over voltage condition, the gate voltage is reduced by shorting the gate voltage via transistor T1 (Column 4 Lines 7-12). Upon modification by Williams, the shorting of this voltage would result in the gate diode being activated and therefore limiting the voltage across the gate resistor/diode parallel pair to the diode's activation voltage. As the voltage of the accumulator is being reduced as a result of

being shorted, it should be easily seen that the voltage supplied to the gate would not be higher than the activation voltage of the diode in combination with the reduced accumulator voltage.

12. In re Claim 12, Gscheidle teaches that the protective circuit is integrated in an ASIC (Column 1 Lines 15-47).

13. In re Claim 13, Gscheidle teaches that the multi-voltage on-board electrical system is a motor vehicle on-board electrical system (Column 1 Lines 15-47).

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER J. CLARK whose telephone number is (571)270-1427. The examiner can normally be reached on M-F, 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CJC
3/19/2008

/Stephen W Jackson/
Primary Examiner, Art Unit 2836